In Iida, et al., G2 (the axial-direction temperature gradient (°C/mm) of the void defect formation temperature region (the temperature region near 1120°C) is not described, and hence G1xG2 is not described as suggested by Iida. The inventions of claims 7-9 herein, use G1xG2 as a parameter. G1xG2 may be described as follows:

The defect density D is expressed by the function (equation (a)) in which the pulling speed V and the temperature gradient G2 are used as parameters.

D = f (VxG2) ... (a)
The R-OSF (OSF ring) inner diameter is determined by V/G1.
$R \propto (V/G1)$ ... (b)

Assuming here that R is a constant condition (e.g., 70% of the diameter), the equation (c) holds from the equations (a) and (b).

a = V/G1 (a: a constant including R)
V = a · G1
D = f (a · G1xG2) ... (c)

The equation (c) is an equation expressing the defect density when the R-OSF inner diameter is constant, in which D is expressed as a function with G1xG2 as a parameter.

The relationship between G1xG2 and the R-OSF inner diameter is shown in Figs. 3(A) to 3(F). Figs. 3(A) to 3(F) are distribution diagrams shown in the numerical data in Table B1 to Table B6 in the specification, in which the axis of abscissa represents G1xG2 and the axis of ordinate represents R-OSF inner diameter/crystal diameter. In the figures, the mark O shows the data with no dislocation clusters at the GOI ration of 60% or higher and the mark ✕ shows that data with no dislocation clusters at the GOI ration of 60% or lower.

As seen from Figs. 3(A) to 3(F), the data (marked O) can be obtained under the conditions of claims 7 and 9. Namely, under the conditions:

$1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$ ... ① (from Figs. 3(B), 3(C) and 3(D))
$0.5 <$ (R-OSF inner diameter/crystal diameter) $< 1.06 \times (G1xG2)^{-0.2}$ ... ②

These conditions ① and ② are the limitations (1) and (2) of claims 7 and 9.

Meantime, the factor "1.06" and the exponent "-0.2" in the above condition ② are the factors of a straight line which divides the GOI ratio of 60% or higher from the GOI ration of 60% or lower, that are obtained by the experiments.

According to the inventions of claims 7 and 9, since G1 and G2 are used as parameters, it is possible to select a manufacturing condition of the crystal with a high oxide-film-withstand-voltage from a wide range of the manufacturing conditions.

Claim 3 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hourai or Iida and in further view of Luter, et al. The Examiner stated that it would have been obvious to modify Hourai or Iida with Luter to avoid undesired changes in the thermal profile during the growth process.

The invention of claim 3 is one in which the "adjustment of a distance between a heat shielding member and a silicon melt" and "change of a temperature gradient" are correlated. Iida, et al. ('264) and Hourai, et al. ('873) simply describe the "adjustment of a temperature gradient", and Luter, et al. ('127) describes the "change of a distance between a heat shielding member and a silicon melt". By combining these inventions, it is impossible to correlate "adjustment of a distance between a heat shielding member and a silicon melt" and "change of a temperature gradient". Therefore, it cannot be said that the invention of claim 3 is obvious over the prior art. According to the invention of claim

3, since the temperature gradient can be changed regardless of the pulling speed, the pulling speed can be set as desired.

Claim 13 has been rejected as being anticipated by Iida, et al. The Examiner states that Iida teaches controlling the ratio of an OSF ring inner diameter to a crystal diameter and the controlling of a temperature gradient at the edge and center and arranged similar to the range taught by Applicant. Further, the Examiner has rejected Claim 13 as being anticipated by Hourai, et al. The Examiner stated that Hourai teaches controlling a ratio of OSF inner ring diameter to a crystal diameter and thermal gradients at the edge and center of an ingot. However, neither Iida nor Hourai teach or suggest the control of G1xG2 and $G1_{edge}/G1_{center}$. As recited in Claim 13, since the temperature gradient can be changed regardless of pulling speed, the pulling speed can be reset as desired.

As claims 8 and 10 depend from claim 7, which has been shown to be patentable above, claims 8 and 10 are also patentable by virtue of their dependency thereon.

Reconsideration and re-examination are respectfully requested.

With the above Amendments and remarks this application is considered ready for allowance and Applicant earnestly solicits an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

No further fee or petition is believed to be necessary in addition to those that are enclosed. Should any fee be needed, please charge our Deposit Account No. 23-0920, and deem this paper to be the required petition.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this Amendment and a Postcard are being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Attention: Box Amendment, Commissioner for Patents, Washington, D.C. 20231, on December 16, 2002.

Gerald T. Shekleton
Gerald T. Shekleton

MARKED UP CLAIMS

1. (Amended) [The] A silicon single crystal ingot production method [according to claim 2, characterized in that] wherein the silicon single crystal ingot production is performed [while] by adjusting a distance between a silicon melt and a heat-shield member installed in a Czochralski-method silicon single crystal production equipment to change a temperature gradient within the crystal in a pulling axis direction.

8. (Amended) A silicon wafer, cut from the silicon ingot of claim 7, [characterized in that] wherein the inner diameter of the OSF ring is at least 1/2 the inner diameter of the wafer and an oxide film withstand the voltage is 60% or higher at a C mode ratio.

10. (Amended) A silicon wafer for non-annealing, cut from [a silicon ingot produced by the CZ method] the silicon ingot of claim 7, wherein [the silicon ingot is produced by pulling under a condition such that "$1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$" and an] the inner diameter of an OSF ring is at least 1/2 a wafer inner diameter and an oxide film withstand voltage is 60% or higher at a C mode ratio.